REMARKS

Status of the Claims

- Claims 1, 4, 6, 9, and 11-13 are pending in the Application after entry of this amendment.
- Claims 1, 4, 6, 9, and 11-13 are rejected by Examiner.
- Claims 1, 4, 6, 9, and 11-13 are amended by Applicant.

Previous Office Action Response

Applicant thanks the Examiner for noting that all claims in Applicant's response dated January 22, 2008 were, in fact, amended. Applicant further amends those claims with proper notation herein.

Claim Rejections Pursuant to 35 U.S.C. §103

Claims 1, 4, 6, and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Profibus Technical Description Order No. 4.002, September 1999, (Profibus) in view of U.S. Patent No. 4,547,849 to Louie et al. (Louie) Applicant respectfully traverses the rejection via amendment.

Independent Claims 1 and 6 are amended to include the aspects of a data transfer that occurs from a central IC to a peripheral IC using start and transfer pulses on a control line. The start pulse is transmitted on the control line when there are transitions on the clock signal and the transfer pulse is transmitted on the control line when there are no transitions on the control line. Applicant finds support for this amendment in the specification on page 7 line 30 through page 9 line 23 and Figure 3 of the present application.

Profibus describes a process field bus having freeze and sync modes. These modes are used in for event-controlled synchronization of slaves operating in a Profibus architecture. Profibus at page 15, col. 2 second paragraph states:

"The slaves begin sync mode when they receive a sync command from their assigned master. The outputs of all addressed slaves are then frozen in their current state. During subsequent user data transmissions, the output data are then stored at the slaves, but the output states remain unchanged. The stored output data are not sent to the outputs until the next sync command is received. Sync mode is concluded with the unsync command." (Profibus, p. 15, col 2).

Thus, in Profibus, the masters send a sync command to the slaves in order to freeze the output states. User data is then sent to the slaves to be stored, and a second sync command is used to transfer the stored data to the slave outputs.

The present Office Action dated 4/30/2008 indicates on page 4 that "...Profibus does not explicitly disclose that it is via the bus connection...having a data line, a control line, and a clock line..." as recited in pending Claim 1. Applicant agrees. However, Applicant respectfully disagrees that Louie discloses the missing elements.

Louie describes an interface between a master microprocessor and a slave coprocessor that is characterized as a nonclock-synchronous interface. (See Louie, col. 1, lines 55-60 and the Abstract). Figure 1 of Louie depicts the bus unit 200 interface between the master microprocessor and the coprocessor 207. The interface lines between the bus unit and the coprocessor include an ADDRESS line 400, a COACK# line 402, a COREQ line 404, a DATA line 406, an ERROR line 408, a BUSY line 410, and CONTROL lines 412. Applicant notes that there are no clock lines. This observation comports with the statement in the Abstract that the interface is a "nonclock-synchronous" interface between the between the microprocessor and the coprocessor. This fundamental aspect differs from the pending claims because the pending claims include a clock line as part of the interface. Pending Claim 1 recites, in relevant part:

"...transmitting the operating parameter from a central IC via a bus connection to the peripheral IC, the bus connection being a serial bus

connection having a data line, a control line, *and a clock line;* ..." (Part of pending Claim 1)

Thus, Louie discloses an interface that operates without a clock line as in the pending claims. However, this is not the only difference between the pending claims and the teachings of Louie. For example, Louie teaches that data is transferred from the slave coprocessor unit to the master microprocessor. This is opposite to the transfer of the pending claims which transfer data from the master to the slave. As taught in Louie at col. 2, lines 24-39:

"Data are transferred from the coprocessor to main memory via the data channel in the following manner. The control logic is responsive to the COREQ signal line for transferring data from the coprocessor to the data register during a first cycle, the data being read from an address in the coprocessors memory corresponding to an address stored in the I/O address register. The transferring means includes means for energizing the COACK# signal line to acknowledge the coprocessor request during the first cycle. Means responsive to the control means, operative during a second cycle, places the read data in the data buffer register on the data bus and places the address in the memory address register on the address bus. This transfers the data to the main memory." (Louie, col. 2, lines 24-39).

Applicant notes that the interface diagram of Louie Figure 2 depicts that the COREQ signal line which starts the transfer originates in the slave coprocessor and is driven to the bus unit of the master microprocessor. This flow is the opposite of the pending claims in which the start pulse originates from the master (central IC) and is sent to the slave (peripheral IC) to transfer data from the master to the slave.

Thus, Louie fails to teach the Claim 1 aspect of "transmitting the operating parameter from a central IC via a bus connection to the peripheral IC" because Louie teaches the opposite; transmitting data from the slave to the master. Louie also fails to teach the Claim 1 aspect of "a serial bus connection

having a data line, a control line, and a clock line" because Louie specifically operates without a clock line. Louie also fails to teach the Claim 1 aspect of "sending a start pulse signaling a start of a data transmission from the central IC to the peripheral IC via the control line" because, in Louie, the slave, not the master, asserts the COREQ signal to start a data transfer. Louie also fails to teach the Claim 1 aspect of "the start pulse is transmitted on the control line during a first phase where transitions of the clock signal are present on the clock line and wherein the transfer pulse is transmitted on the control line in a second phase where transitions of the clock signal are not present on the clock line" because Louie fails to describe a clock line as part of a serial bus connection. Independent Claim 6 has similar features which Louie fails to describe.

Since Louie fails to describe aspects of amended independent Claims 1 and 6 which are not described in Profibus, then the combination of Profibus and Louie fails to render obvious the amended Claims 1 and 6 under 35 USC §103(a) as well as their dependent Claims 4, 9, and 11-13 per MPEP §2143.03. In addition, Louie teaches away from the pending claims because Louie specifically discloses a "nonclock" interface between a master and a slave. The pending claims recite a serial bus that includes a click line. Thus, the combination of Profibus and Louie cannot teach or suggest all of the elements of the pending claims and cannot form a prima facie case of obviousness under 35 USC §103(a).

Applicant respectfully requests reconsideration and withdrawal of the 35 USC §103(a) rejections on Claims 1, 4, 6, and 9 in light of the amendments and the arguments presented above.

Claims 11-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Profibus Technical Description Order No. 4.002, September 1999, (Profibus) in view of U.S. Patent No. 4,547,849 to Louie et al. (Louie) and

in further view of U.S. Patent No. 7,120,427 to Adams et al. (Adams). Applicant respectfully traverses the rejection via amendment of independent Claim 6.

The teachings of Profibus and Louie are presented above. Applicant notes that the combination of Profibus and Louie fails to establish a prima facie case of obviousness against pending amended independent Claim 6, upon which Claims 11-13 depend, because the combination of Profibus and Louie fails to teach or suggest all of the elements of independent Claim 6 and the combination actually teaches away from the claimed invention. The addition of Adams to the combination of Profibus and Louie does not change that result. Adams fails to teach the elements missing from the combination of Profibus and Louie. Adams also cannot cure the aspect that the nonclock interface of Louie teaches away from the pending claims. Accordingly, Claims 11-13 are not rendered obvious by the combination of Profibus, Louie, and Adams per MPEP §2143.03.

Applicant respectfully requests reconsideration and withdrawal of the 35 USC §103(a) rejections on Claims 11-13 in light of the amendment to independent Claim 6 and the arguments presented above.

Conclusion

Applicant respectfully submits that the amended pending claims patentably define over the cited art and respectfully requests reconsideration and withdrawal of all rejections of the pending claims.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 07-0832 therefore.

Respectfully submitted,
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